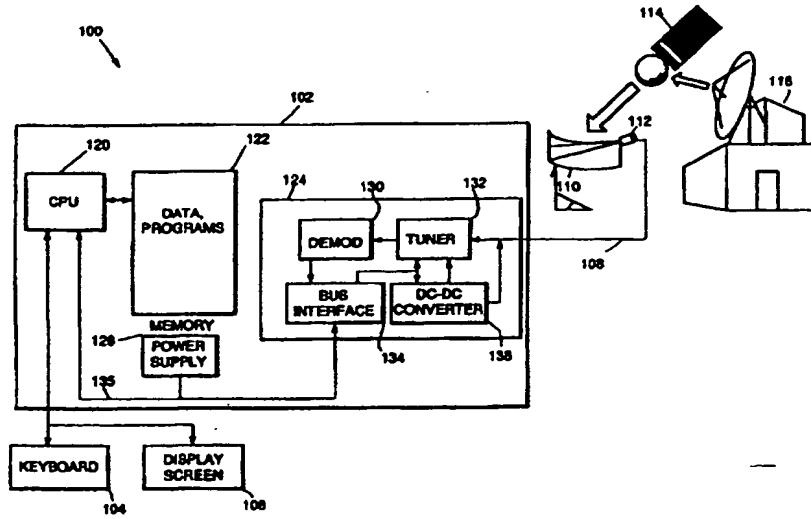




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## (54) Title: SATELLITE RECEIVER COMPUTER ADAPTER CARD



## (57) Abstract

A printed circuit board intended to be placed within a card slot of a personal computer (102) that allows the personal computer (102) to receive information directly from a satellite communication network. An adapter card (124) operates in slave mode to a CPU (120) of the personal computer (102). The CPU (120) receives demodulated signals from a demodulator (130) of the adapter card (124) via a bus interface (134) on the adapter card (124). The CPU (120) also receives status information for the demodulator (130) and a tuner (132) and controls the operations of the demodulator (130) and tuner (132) via the bus interface (134). A DC-DC converter (136) receives power from a power supply (126) for the adapter card circuitry. Moreover, the DC-DC converter (136) powers a low noise block (LNB 112) of an antenna (110) of the satellite communication network.

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Description

## SATELLITE RECEIVER COMPUTER ADAPTER CARD

Background of the Invention

5 This application relates to a computer network and, more specifically, to a method and apparatus for an adapter card for a personal computer that receives information transmitted from a satellite.

In conventional satellite communication networks a hub station sends signals to a satellite and then to a receiver on the ground. The receiver includes an antenna. The antenna contains a 10 low noise block (LNB) that amplifies and down converts an entire received transmission to L-band (typically 950 MHz to 1450 MHz) and passes the resulting signal into an interfacility link (IFL). The IFL is typically a coaxial cable that carries power to the LNB and carries the L-band signal to an Indoor Unit (IDU). The L-band coaxial cable is a standard interface in the satellite communications industry and is normally used regardless of the actual satellite transmission band (C-band, Ku-band, etc.).

15 The IDU is a separate unit that contains a power supply for the LNB and for the IDU. The IDU also contains a tuner, demodulator, and a controller. The controller selects the tuner's frequency, the demodulator's bit rate, and performs various other functions needed for the operation of the receiver. The IDU tuner receives all of the signals from the satellite and selects a single signal for 20 reception. The selected signal is passed to the demodulator. The IDU demodulator converts the analog signal from the tuner back into a digital data stream and passes it to an output line of the IDU.

The output line of the IDU is typically input to a serial adapter card in a personal computer. The serial adapter card allows the digital data stream to be processed by the computer and allows the computer to communicate with the controller to control the operation of the satellite receiver.

25 A disadvantage of such conventional systems lies in the fact that the IDU is a separate unit that is remote from the personal computer. Thus, the IDU, which is typically incorporated into the receiver unit, adds additional components to a satellite communication network. Such additional components increase the packaging requirements of the system. In addition, a separate cable is required to connect the IDU to the serial adapter of the computer.

Disclosure of the Invention

30 The present invention overcomes the problems and disadvantages of the prior art by placing a printed circuit board within a personal computer that allows the personal computer to receive information directly from a satellite without having to incorporate a separate unit between the personal computer and the receiving antenna for the demodulating and tuning functions. This information can

include a digital video signal, a digital audio signal, a broadcast file transfer, or any other desired information transfer.

The present invention eliminates the need for a separate controller, such as the controller contained in a conventional IDU, because the personal computer can perform control functions.

5 Furthermore, the reduction of circuitry achieved by applicant's invention increases the reliability of the system.

The present invention includes a DC-DC converter that transmits power from the power supply of the personal computer to the LNB of the antenna. Moreover, the circuitry of the applicants' personal computer adapter card can be powered by the power supply of the personal computer.

10 In accordance with the purpose of the invention, as embodied and broadly described herein, the invention is an adapter card in a personal computer having a CPU for connecting the personal computer to a satellite communication network, comprising: a connector for receiving a plurality of analog signals from the satellite communication network; a tuner, connected to the connector, that receives the plurality of analog signals from the connector and selects a single analog signal for 15 reception; a demodulator, connected to the tuner, that converts the analog signal from the tuner into a digital data stream; and a bus interface, connected to the demodulator and the CPU, that allows the CPU to request the digital data stream from the demodulator.

20 In further accordance with the purpose of the invention, as embodied and broadly described herein, the invention is an adapter card in a personal computer having a CPU for connecting the personal computer to a satellite communication network, comprising: a connector for receiver for receiving a plurality of analog signals form the satellite communication network; a tuner, connected to the connector, that receives the plurality of analog signals from the connector and selects a single analog signal for reception; a demodulator, connected to the tuner, that converts the analog signal from the tuner into a digital data stream; and a bus interface, connected to the tuner, the demodulator, and the 25 CPU, that allows the CPU to send commands to the tuner and the demodulator to control operation of the tuner and the demodulator.

30 In further accordance with the purpose of the invention, as embodied and broadly described herein, the invention is an adapter card in a personal computer having a CPU and a power supply for connecting the personal computer to a satellite communication network, comprising: a connector for receiver for receiving a plurality of analog signals from the satellite communication network; a tuner, connected to the connector, that receives the plurality of analog signals from the connector and selects a single analog signal for reception; a demodulator, connected to the tuner, that converts the analog signal from the tuner into a digital data stream; a DC-DC converter; a bus interface, connected to the demodulator, the tuner, the CPU, and the power supply that allows the CPU to send and

receive data to and from the adapter card and that allows voltage from the power supply to be sent to the DC-DC converter.

In further accordance with the purpose of the invention, as embodied and broadly described herein, the invention is a method for controlling an adapter card in a personal computer having a CPU, for connecting the personal computer to a satellite communication network, comprising the steps of: receiving, by the adapter card, a plurality of analog signals from the satellite communication network; selecting, by the adapter card, a single analog signal for reception; converting, by the adapter card, the analog signal into a digital data stream; receiving, by the CPU, commands to the tuner of the adapter card and to the demodulator of the adapter card via the bus interface to control operation of the tuner and the demodulator in accordance with the status information.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

#### Brief Description of the Drawings

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Fig. 1 is a hardware block diagram of a preferred embodiment of the invention;

Fig. 2 is a diagram showing additional detail of a satellite receiver computer adapter card of Fig. 1;

Fig. 3 is a block diagram showing additional detail of the satellite receiver computer adapter card of Fig. 2;

Fig. 4 is a diagram of steps performed by a CPU of Fig. 1; and

Figs. 5(a) through 5(f) are detailed diagrams of steps performed by the CPU of Fig. 1 during tuning and demodulation.

#### Detailed Description of the Preferred Embodiments

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

Fig. 1 is a hardware block diagram 100 of a preferred embodiment of the invention connected to a satellite communications network. Fig. 1 includes a personal computer 102, a keyboard 104, a display screen 106, an IFL link 108, an antenna 110, an LNB 112, a satellite 114, and a hub 116. Personal computer 102 includes a CPU 120, a memory 122, a satellite receiver computer adapter card 124, a bus 135, and a power supply 126. The personal computer also includes one or more expansion

slots (not shown) into which an adapter card such as the adapter card 124 can be plugged. Adapter card 124 includes a demodulator 130, a tuner 132, a bus interface 134, and a DC-DC converter 136.

IFL 108, antenna 110, LNB 112, satellite 114, and hub 116 are all of a known type. Hub 116 preferably sends a signal in a Ku-band having approximately a 500 MHz frequency range to satellite 114. The signal preferably is encoded using Binary Phase Shift Keying (BPSK) but could be encoded using other methods. Satellite 114 transmits the signals to a receiver including antenna 110. The signal from the hub can be any desired signal such as a digital video signal, e.g., MPEG-1 or INDEO 3.2, a digital audio signal, e.g., ADPCM, or a broadcast file transfer. Antenna 110 contains a low noise block (LNB) 112 that amplifies and down converts an entire received transmission preferably to L-band (typically 950 MHz to 1450 MHz) and passes the resulting signal into an interfacility link (IFL) 108. IFL 108 is preferably a coaxial cable that carries power from the DC-DC converter 136 to LNB 112 and data from LNB 112 to tuner 132.

Adapter card 124 is connected to CPU 120 via bus 135. Bus 135 is connected to adapter card 124 via bus interface 134. Bus 135 can be, e.g., an IS, EISA, or Microchannel bus, or any other bus well known in the art. Bus interface 134 is a suitable bus interface of a type corresponding to a type of bus 135. Bus 135 and bus interface 134 also can be other types of busses or bus interfaces suitable for use with the present invention.

Memory 122 includes data and software programs. CPU 120 executes the instructions of the software programs to perform the steps in a conventional manner. CPU 120 preferably is a 33 MHz or faster Intel 486 microprocessor belonging to the X86 family of microprocessors, manufactured by Intel Corp., but may be any similarly capable CPU depending upon the nature of the personal computer.

Adapter card 124 preferably is a single printed circuit board that fits into a card slot in personal computer 120. Within the adapter card 124 tuner 132 receives the plurality of analog signals via IFL 108. Tuner 132 selects one of the analog signals in accordance with a tuning frequency previously sent to tuner 132 by CPU 120. Tuner 132 passes the selected signal to demodulator 130, where it is demodulated and passed to CPU 120 of computer 102 via bus interface 134. The adapter card 124, including the connector, the tuner 132, the demodulator 130 and the bus interface 134, is powered by power supply 126. Power supply 126 also powers all components in computer 102 and LNB 112. The voltage signal is also sent from DC-DC converter 136 to LNB 112 via IFL 108.

Fig. 2 is a diagram showing additional detail of the preferred embodiment of adapter card 124. Adapter card 124 also preferably includes a Forward Error Correction (FEC) Level 2 element 140 and an FEC Level 1 element 142, bus interface 134, a receiver (Rx) controller 146, and a

microprocessor 148. FEC elements 140 and 142 and microprocessor 148 are optional and may be omitted in certain implementations of the invention.

Rx controller 146 provides a packet framing function, address filtering, which allows simultaneous reception of approximately 100 addresses and Data Encryption Standard (DES) decryption. Additional details of adapter card 124 of Fig. 2 are discussed below in connection with Fig. 3.

Fig. 3 is a block diagram showing additional details of adapter card 124. Microprocessor 148 is omitted from the embodiment of Fig. 3. In Fig. 3, the received signal is received at tuner 132 via IFL 108 and is passed to demodulator 130 for demodulation. The data is forward error corrected in FEC elements 140 and 142 and is passed to CPU 120, via bus interface 134. In Fig. 3, bus 135 is preferably an ISA bus, although bus 135 may be any suitable bus. The ISA implementation of adapter card 124 shown in Fig. 3 preferably operates in "slave mode." That is, received data is buffered in a 64K RAM 160 until CPU 120, sends a request for data to adapter card 124 via bus 135. In implementations using a Microchannel bus, RAM 160 is replaced by a 64K byte FIFO buffer. Received data preferably is encoded using a BPSK format.

Tuner 132 preferably is a known tuner of a type manufactured by Sharp or Panasonic. Demodulator 130 can be any known type of demodulator. Preferably, demodulator 130 is a demodulator of a type found in the DirecTv product, of a type found in the RCA DSS satellite receiver sold by Thomson Consumer Electronics, Inc. Demodulator 130 includes a voltage controlled oscillator (VCO) 162, a low pass filter (LPF) 163, and A/D converter 164, an amplifier 166, an automatic gain control (AGC) element 168, an automatic frequency control (AFC) element 170, a D/A converter 172, an application specific integrated circuit (ASIC) 174, and a depuncture logic element 176.

FEC elements 140 and 142 function to correct one bit errors using a known method. For example, FEC may be implemented via Stanford Telecom (STEL) or HNS Viterbi decoding. In the preferred embodiment, a Reed-Solomon decoder 178 corrects multi-bit errors. Both the FEC elements and Reed-Solomon decoder 178 are optional and may be deleted from some implementations of the present invention.

Rx controller 146 of Fig. 3 performs frame detection on the received, demodulated, error-corrected signal. Frame detection includes functions such as address recognition, CRC checking, maximum frame length checking, and frame error detection.

Rx controller 146 additionally performs DES decryption in implementations of the invention where the incoming signal is encrypted. In still other implementations, Rx controller 146 performs address filtration so that only data of interest will be passed to CPU 120, shown in Fig. 1.

Other implementations of the invention use a known high-level data link control (HDLC) element in place of Rx controller 146, such as the Z85C30 HDLC manufactured by Advanced Micro Devices.

DC-DC converter 136 includes two voltage regulator (VR) elements 180 and 182. DC-DC converter 136 preferably receives a 5V signal from the power supply 126, shown in Fig. 1, supplied by bus 135 via bus interface 134 and outputs a 15V and a 21V signal, although it may instead receive a 12V signal from the power supply 126 for conversion. The 15V signal and the 21V signal both are input to tuner 132. In a preferred embodiment, the 21V signal is passed from tuner 132 to LNB 112 to provide power to LNB 112. The LNB requires a 15V signal, but the tuner sends a 21V signal to account for losses in the IFL 108.

Fig. 4 is a diagram of steps performed by CPU 120, as shown in Fig. 1. In addition to the steps shown in Fig. 4, CPU 120 performs the functions normally performed by a CPU of a personal computer. CPU 120 also processes the packets received by adapter card 124. As shown in Fig. 4, and referring back to Fig. 1, in step 402 CPU 120 sends signals to tuner 132 via bus 135 and bus interface 134. In the described embodiment, shown in Fig. 3, signals pass to tuner 132 through demodulator ASIC 174. Thus, when a person indicates a tuning frequency via, e.g., keyboard 104 or a touch display in display screen 106, CPU sends data that is passed to tuner 132 on data line 191. Specifically, CPU 120 sends a one-bit enable signal to tuner 132 on line 192. Then, approximately every 18 msec (in response to a real time interrupt signal) CPU 120 toggles clock line 190 and sends one bit of the tuning frequency to tuner 132. Clock line 190 is toggled and a bit sent every 18 msec until the tuning frequency has been sent. In one implementation, a graphical user interface (GUI) makes it easy for a person to enter a tuning frequency. In other implementations CPU 120 plays a sound over a speaker (not shown) when the demodulator and FEC element are locked. In still other implementations, CPU 120 may determine a tuning frequency without human intervention.

In step 404, CPU 120 checks the quality of the signal received from demodulator 130. Signal quality is preferably measured by Signal Quality Factor (SQF) and Energy Per Bit to Noise Ratio (EBNR). These details are determined by the adapter card hardware and software and the operating system of the operating computer. In step 406 CPU 120 sends a signal to point the antenna in accordance with the quality of the received signal. In step 408, if demodulator 130 and FEC 140/142 are not locked, the tuning frequency is adjusted in step 410 as described below and steps 402 and 408 are repeated.

In the preferred embodiment, the tuner 132 is able to tune within plus or minus 2 MHz of the correct signal frequency. In order to begin receiving, i.e., to acquire or lock the signal, the adapter card 124 must search through this 4 MHz range.

Figs. 5(a) through 5(f) are diagrams of steps performed by CPU 120, as shown in Fig. 1, for tuner and demodulator control. In the described embodiment, a real time clock interrupt occurs every 18 msec. When an interrupt occurs in step 502, CPU 120 performs miscellaneous processing in step 504. If no tuning frequency has been indicated in step 506, then a tuning frequency is acquired 5 from an operator and an initial state is set to S0 in step 508. Next, control branches depending on a current control state. All branches return to step 510, where a current SQF value is stored in a memory of computer 102.

State S0 is an initial state for channel acquisition. If the current state is S0, i.e., if tuner 10 132 has not been set, then control passes to step 512 of Fig. 5(b). In step 512, CPU 120 programs tuner 132 as described above and sets a current state to S1.

If the current state is S1, CPU 120 configures demodulator 130 at the tuning frequency by sending data, address, and control signals to demodulator 130. Demodulator 130 preferably sweeps 15 in 100 KHz steps for 20 msec in a 4 MHz band. At the end of the sweep, demodulator 130 has determined an SQF value. If the SQF is the best SQF yet, i.e., if it is the highest numerical value, it is saved in step 518. If CPU 120 determines that it is through sweeping through the 4 MHz, then the CPU 120 proceeds immediately to step 510 to store the SQF value and exit the interrupt. If the CPU 120 determines that the sweep through the 4 MHz is not complete, then the CPU 120, in step 522, saves the best SQF found as yet. In step 524 the current state is set to S2 and step 526 the SQF register in demodulator 130 is cleared.

20 When the current state is S2, the CPU 120 sends a command to the demodulator 130 to enable the bit timing recover (BTR) loop. The BTR allows the demodulator 130 to determine where each bit begins and ends and so to correctly sample and demodulate the bits. The command is sent over the data, address, and control lines. After the BTR is enabled, the current state is set to S3.

When the current state is S3, if the FEC lock signal from the Reed-Solomon decoder 25 178 is low in step 530, indicating that the FEC is in lock, i.e., the Reed-Solomon decoder 178 has detected too many errors in transmission from the satellite, CPU 120 in step 532 changes the configuration of demodulator 130. Some factors changed include the length of the frequency sweep, the range of the sweep, and how often sampling is done. The current state is then set to S5 in step 543. If the FEC signal was high in step 530, indicating that there were not too many errors in transmission from 30 the satellite, then control passes immediately to step 510 to store the SQF value and exit the interrupt.

When the current state is S4, the CPU 120 determines if the FEC is in lock and if the demodulator is out of lock. In the preferred embodiment, the CPU 120 determines if the FEC is in lock by reading the FEC lock signal from a register (not shown) in the demodulator ASIC 174 and determining if the FEC lock signal is high, i.e., not locked. This occurs if the Reed-Solomon decoder

178 has detected a large number of errors. The FEC lock signal in the register parallels the FEC lock signal being high if the FEC lock signal is high and being low if the FEC lock signal is low. In the preferred embodiment, the CPU 120 determines if the demodulator 174 is out of lock by reading information from a register in the demodulator indicating whether the modulator is out of lock.

5 If the FEC is not locked in step 550, i.e., few or no errors are detected by the Reed-Solomon decoder 178, the CPU 120 reads the SQF in step 552 and saves the frequency offset in step 556. If the FEC is locked, the CPU 120 determines if the demodulator 174 is out of lock in step 558. If the demodulator is out of lock, the current state is set to S1. If the demodulator is not out of lock, the current state is set to S3.

10 In summary, the present invention allows a personal computer to be connected to a satellite communication network by merely adding an adapter card to the personal computer and by loading control software into the personal computer. The CPU of the personal computer provides a control function for the adapter card and the power supply of the computer powers both the adapter card and an LNB element connected to the computer. The adapter card accesses the satellite communication  
15 network through a standard IFL. In addition, the reduction of circuitry achieved by applicant's invention increases the reliability of the system.

15 Other embodiments will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope of the invention being indicated by the  
20 following claims.

CLAIMS

1. An adapter card for use in a personal computer, enabling the personal computer to receive a signal from a satellite communication network, comprising:

5

a connector for receiving a plurality of signals from the satellite communication network;

10 a tuner, connected to the connector, that receives the plurality of signals from the connector and selects a single signal for reception;

a demodulator, connected to the tuner, that converts the selected signal from the tuner into a digital data stream; and

15 a bus interface, connecting the adapter card and the personal computer, that allows the digital data stream, a demodulator status and a tuner status to be transmitted from the adapter card to the personal computer.

2. The adapter card of Claim 1, wherein the bus interface allows the personal computer to 20 send commands to the tuner and to the demodulator, to control operation of the tuner and the demodulator.

3. The adapter card of Claim 1 or 2 further comprising at least one forward error correction element for performing a forward error correction on the digital data stream.

25

4. The adapter card of Claims 1, 2 or 3, further including means for performing packet framing on the demodulated signal.

5. The adapter card of Claims 1, 2, 3 or 4, further including means for performing address 30 filtering to receive only predetermined addresses.

6. The adapter card of Claims 1, 2, 3, 4, or 5, further including means for performing decryption on the received signal.

7. The adapter card of Claims 1, 2, 3, 4, 5 or 6, wherein the adapter card is powered by a DC-DC converter connected to a power supply of the personal computer.

8. An adapter card for use in a personal computer for enabling the personal computer to receive a signal from a satellite communication network, comprising:

5 a connector for receiving a plurality of signals from the satellite communication network;

10 a tuner, connected to the connector, that receives the plurality of signals from the connector and selects a single signal for reception;

15 a demodulator, connected to the tuner, that converts the selected signal from the tuner into a digital data stream;

15 a bus interface, connecting the adapter card and the personal computer, that allows the digital data stream from the demodulator to be transmitted to the personal computer; and

20 a DC-DC converter connected to a power supply of the personal computer to provide power for an LNB element of the satellite communication network.

9. The adapter card of Claim 8, wherein the satellite communication network includes an interfacility link and wherein the power is provided from the DC-DC converter to the LNB element via the interfacility link.

25

10. The adapter card of Claim 9, wherein the interfacility link is a coaxial microwave band interface.

30 11. The adapter card of Claims 8, 9 or 10, wherein the DC-DC converter is connected to the tuner and supplies power at a second voltage level to the tuner.

12. A method for controlling an adapter card for use in a personal computer for enabling the personal computer to receive a signal from a satellite communication network, comprising the steps of:

receiving by the adapter card, a single signal from among the plurality of signals for reception;

converting by the adapter card, the signal into a digital data stream;

5

transmitting by the adapter card, the digital data stream, status information from a tuner of the adapter card, and status information from a demodulator of the adapter card to the personal computer via a bus interface.

10 13. The method of Claim 12 further comprising the steps of:

sweeping through a given bandwidth in steps of a smaller bandwidth:

15

calculating at each step a signal quality factor for the received signal:

15

determining if the signal quality factor for the received signal is more desirable than previously calculated signal quality factors; and

20

saving the signal quality factor if it is more desirable.

14. The method of Claims 12 or 13 further comprising the step of receiving, by the adapter card, commands to the tuner and to the demodulator via the bus interface for controlling operation of the tuner and the demodulator in accordance with the status information of the tuner and the demodulator.

25 15. The method of Claims 12, 13 or 14, further comprising the step of obtaining power, by  
the adapter card, from a power supply of the personal computer.

16. The method of Claims 12, 13, 14 or 15, wherein the adapter card comprises a DC-DC converter for providing the further steps of:

30

receiving a voltage signal from the power supply:

converting the voltage signal into a converted voltage signal having a different voltage level; and

supplying the converted voltage signal to the tuner.

17. The method of Claim 16, wherein the DC-DC converter includes a plurality of voltage  
5 regulator elements for providing the further steps of:

converting the voltage signal, by a first voltage regulator element, into a first voltage  
signal providing power of a first voltage to the tuner; and

10 converting the voltage signal, by a second voltage regulator element, into a second  
voltage signal providing power of a second voltage to the tuner.

18. The method of Claim 17, wherein the first voltage is different from the second voltage.

15 19. The method of Claims 15, 16, 17 or 18, further comprising the step of supplying power  
through the tuner to the LNB element.

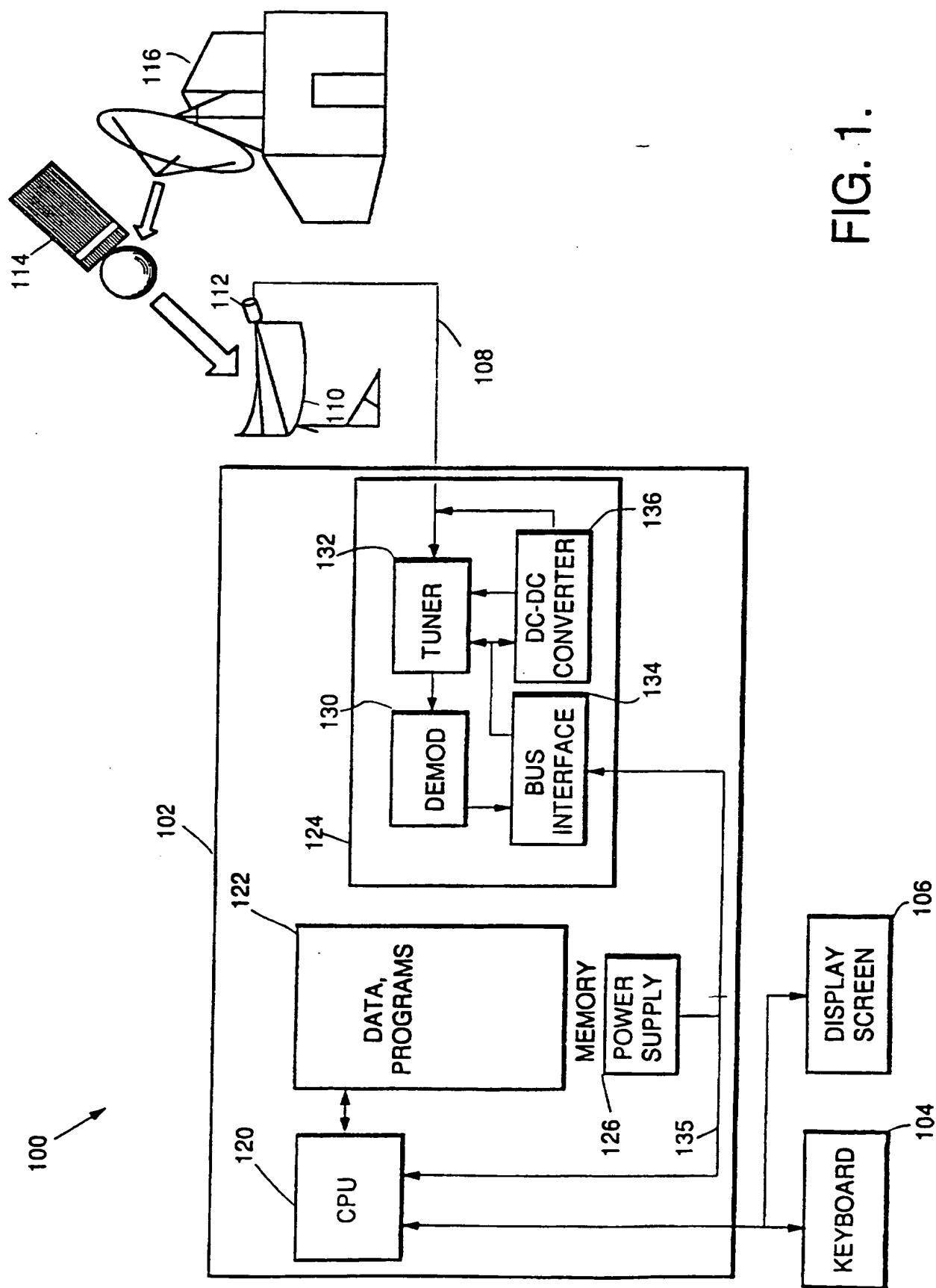
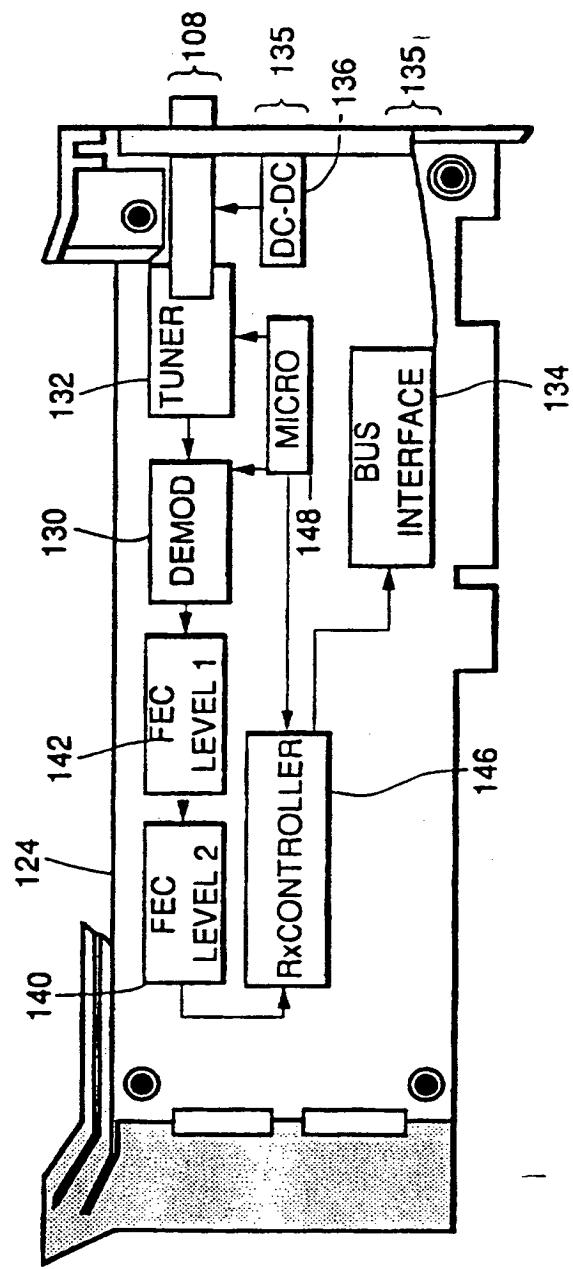
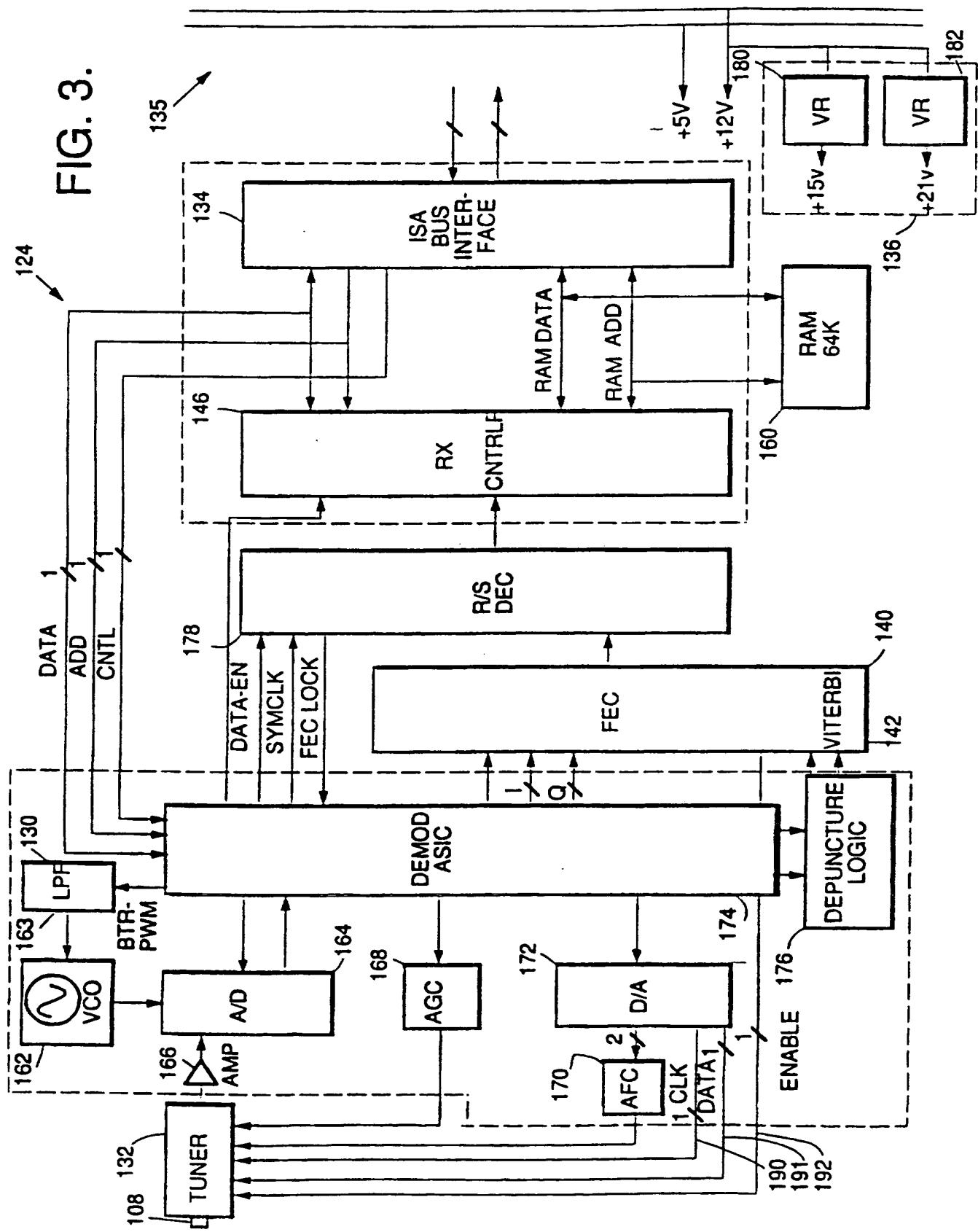


FIG.2.



3  
FIG



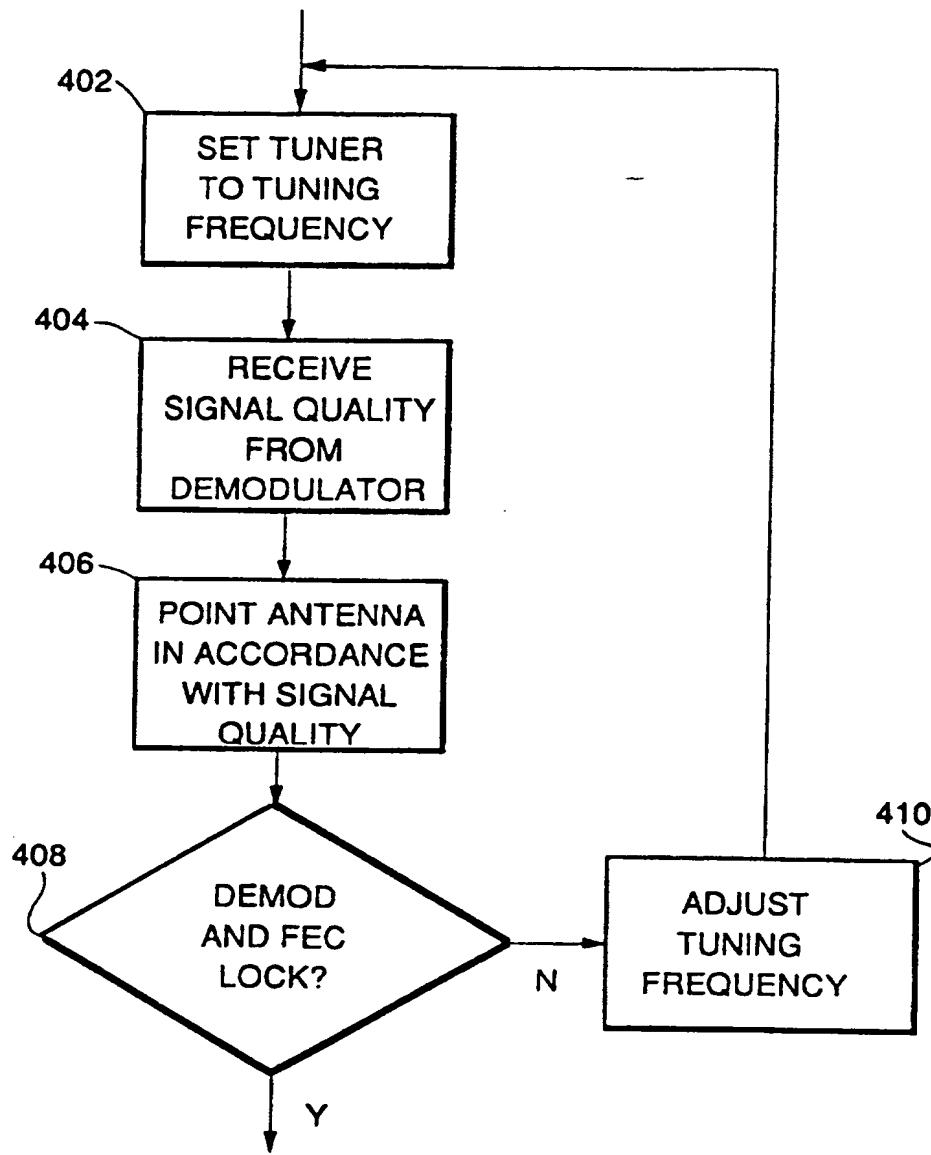


FIG. 4.

FIG. 5a.

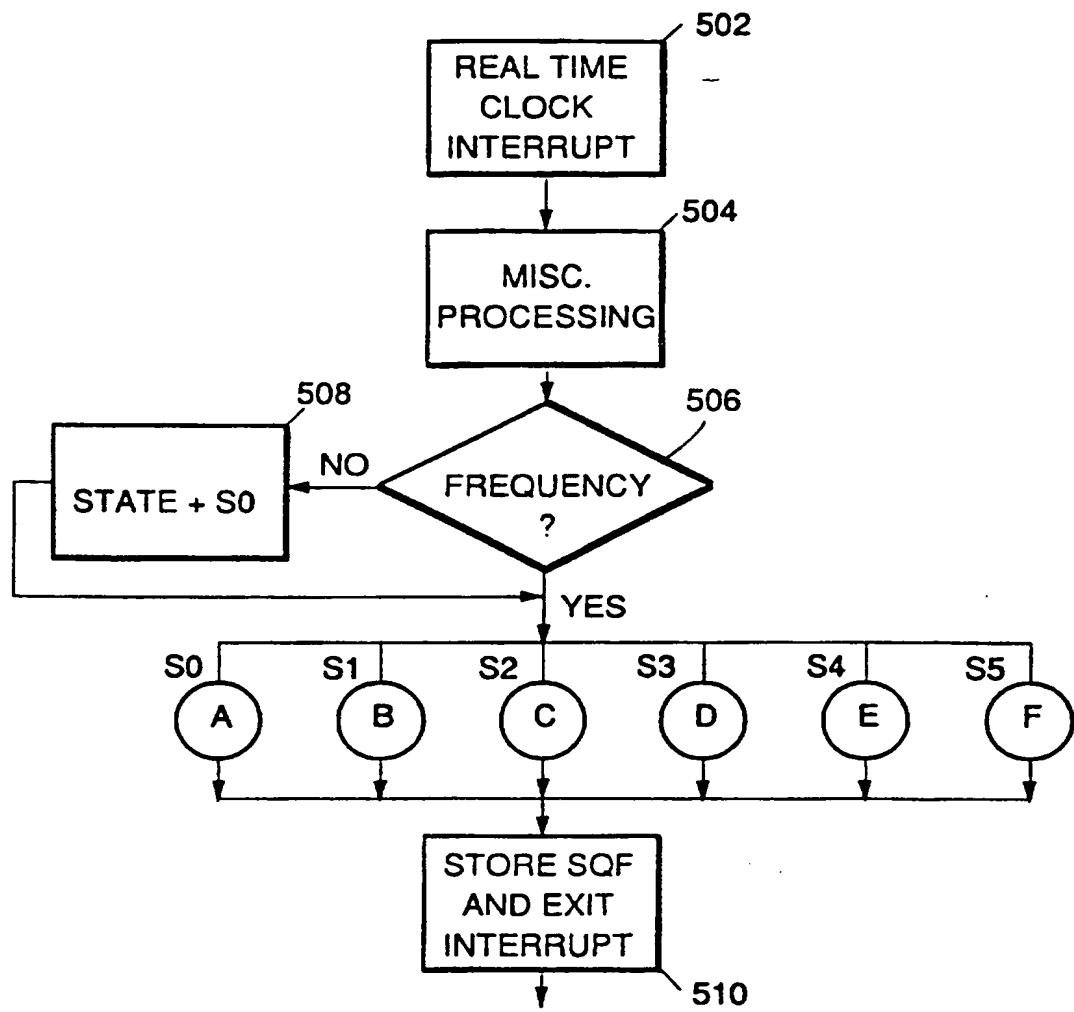


FIG. 5b.

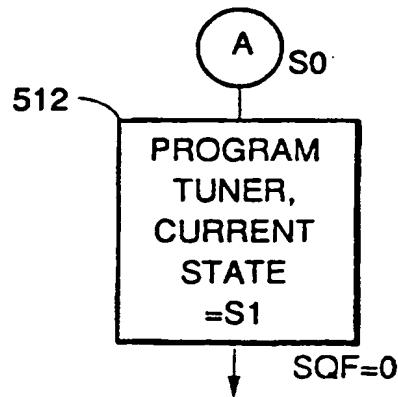


FIG. 5c.

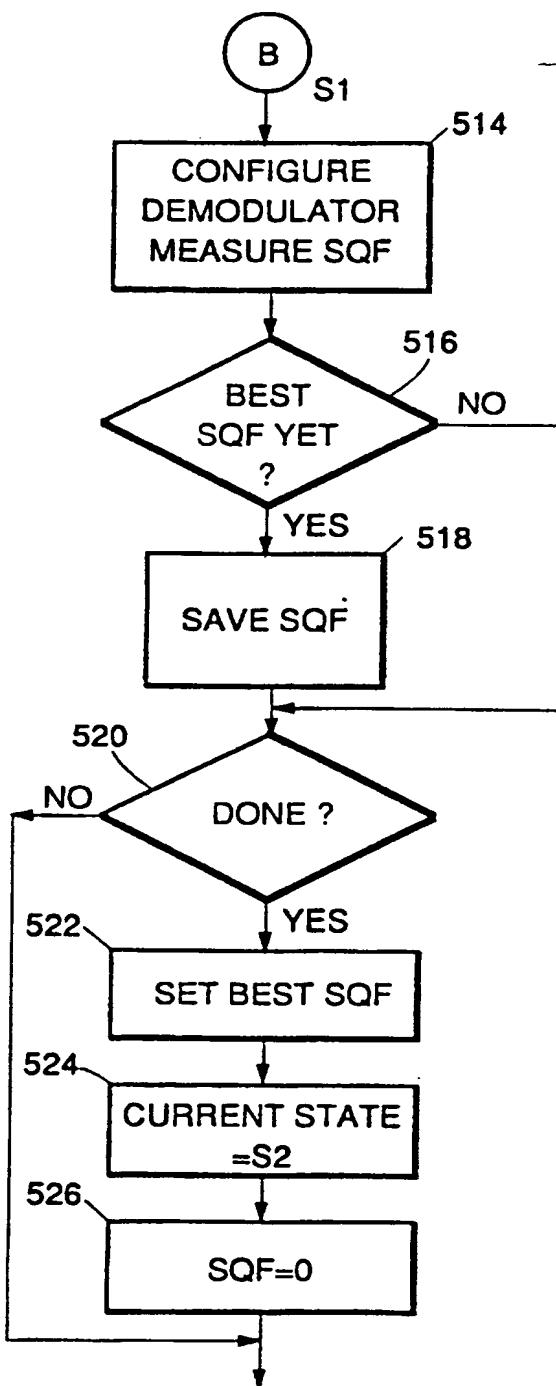


FIG. 5d.

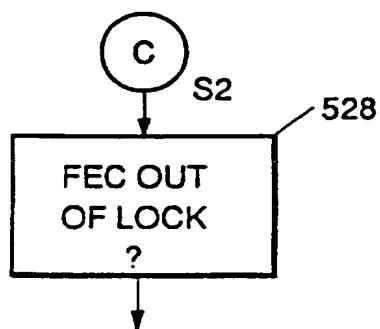


FIG. 5e.

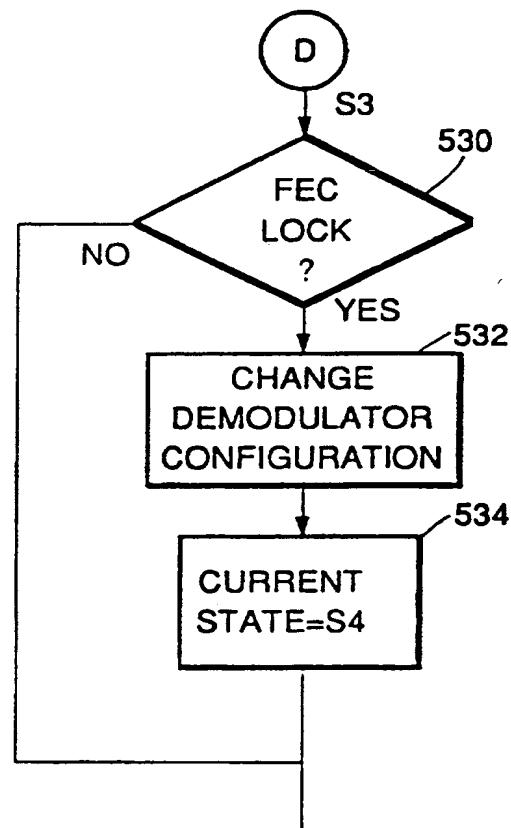
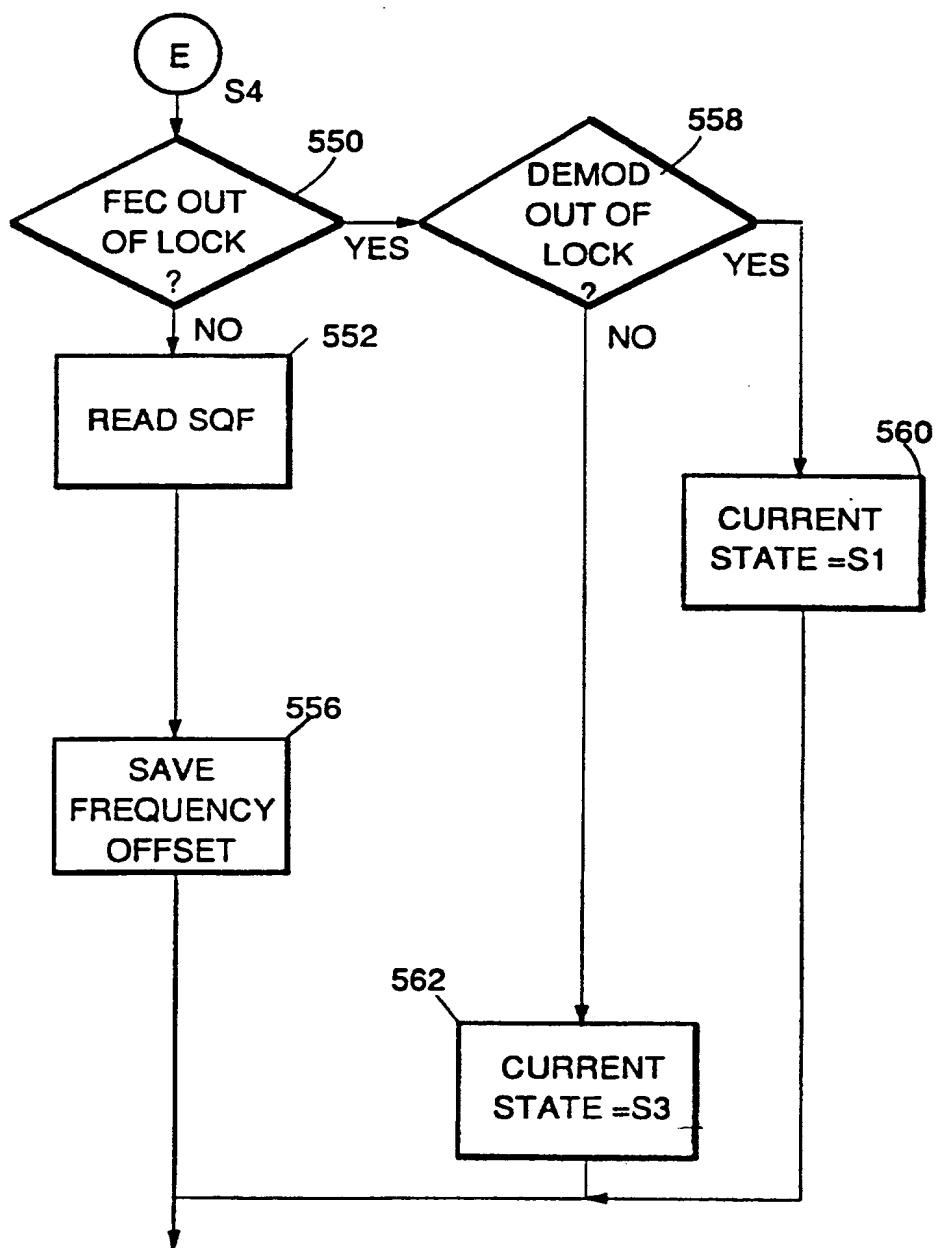


FIG. 5f.



## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US96/00061

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H04N 7/08, 5/46; H04B 1/18  
US CL : 395/282

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/282, 283; 455/186

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,245,429 (VIRGINIO ET AL) 14 September 1993, col. 1, lines 30-60.	1-3, 8-14
X	US, A, 5,359,367 (STOCKILL) 25 October 1994, col. 1, line 16 to col. 3, line 61.	1-3, 8-14

 Further documents are listed in the continuation of Box C.  See patent family annex.

• Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
• "A" document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
• "E" earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
• "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
• "O" document referring to an oral disclosure, use, exhibition or other means		
• "P" document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

26 JULY 1996

Date of mailing of the international search report

17 SEP 1996

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
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INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US96/00061

**B. FIELDS SEARCHED**

Electronic data bases consulted (Name of data base and where practicable terms used):

APS, MAYA

Search terms: adapter card, tuner, demodulator, satellite communication